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U.S. UTILITY Patent Application

PATENT NUMBER and
ISSUE DATE

APPL NUM 10067819	FILING DATE 02/08/2002	CLASS 324 714	SUBCLASS 724	GAU 2133 2858	EXAMINER <i>Beardy</i>
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**APPLICANTS: Matsubara Takayuki; Shimamura Akimitsu;
K3D *KEVERUS*

**CONTINUING DATA VERIFIED: *none*
in 6/4/2004

** FOREIGN APPLICATIONS VERIFIED: *YES 6/4/2004*
JAPAN 2001-136938 05/08/2001
in

PG-PUB	DO NOT PUBLISH <input type="checkbox"/>	RESCIND <input type="checkbox"/>
Foreign priority claimed	<input checked="" type="checkbox"/> yes <input type="checkbox"/> no	ATTORNEY DOCKET NO
35 USC 119 conditions met	<input checked="" type="checkbox"/> yes <input type="checkbox"/> no	60188-150
Verified and Acknowledged Examiners's initials <i>in</i>		
TITLE : Integrated circuit and testing method for integrated circuit		
U.S. DEPT. OF COMM./PAT. & TM.-PTO-436L (Rev. 12-94)		

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G.
Assistant Examiner		DRAWING	
		Sheets Drwg.	Figs. Drwg.
Amount Due		Print Fig.	
Date Paid			
Primary Examiner		Application Examiner	
PREPARED FOR ISSUE			
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